REMARKS

Claims 6-10, 17, and 20 were presented for examination and were pending in this application. In an Office Action dated May 19, 2004, claims 6-10, 17, and 20 were rejected. Applicant thanks Examiner for examination of the claims pending in this application and addresses Examiner's comments below.

Applicant starts by noting that the Specification has been amended to correct grammatical and typographical errors. Entry of these amendments is requested as they do not add new matter and are ministerial in nature. As for the claims, Applicant herein amends claims 6-10, 17 and 20. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments, Applicant has not and does not narrow the scope of the protection to which Applicant considers the claimed invention to be entitled and does not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicant reserves the right to pursue such protection at a later point in time and merely seeks to pursue protection for the subject matter presented in this submission.

Based on the Amendments herein and the following Remarks, Applicant respectfully requests that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Rejection Under 35 USC § 112, Paragraph 2

In the 2nd paragraph of the Office Action, Examiner has rejected claims 6-10, 17, and 20 as allegedly not specifically pointing out and distinctly claiming the subject matter that the Applicant regards as the invention.

Applicant has amended claim 6 to provide appropriate antecedent basis, specifically reciting "plurality of ordered incoming packets." In addition, claim 8 has also been amended to now recite "plurality of ordered incoming packets" to provide proper antecedent basis. Therefore, the basis of the rejection based on antecedent basis is now obviated and removal of the rejection on this basis is requested.

As for ordering of the steps, Applicant respectfully submits that the steps require no specific order and the claimed invention is operational when either processing or pre-processing occurs first in a sequence. However, to address Examiners concerns in instances when ordering was to include pre-processing followed by processing, Applicant begins by noting that the claim recites:

> pre-processing each of the plurality of ordered incoming packets to determine whether processing on a previous packet is in progress, the previous packet comprising at least a portion of the micro-flow . . . .

Thus, the claimed invention undertakes a pre-processing step for the plurality of ordered incoming packets to determine if previous packets from the same micro-flow are being processed. Thereafter, the claimed invention recites:

> processing each of the plurality of ordered incoming packets on the a processor of the plurality of processors to which the ordered incoming packet is assigned, in response to completion of processing of the previous packet.

Thus, the claimed invention processes each of the plurality of ordered incoming packets once processing of the previous packet completes. Therefore, the claim recites an operable process of pre-processing incoming ordered packets and then processing the ordered

incoming packets once previous packets of the same micro-flow have been processed. Applicant respectfully submits the claim is understandable and functional accordingly, and therefore, the basis of the rejection based on this concern is now obviated. Removal of the rejection on this basis is requested.

Likewise, the basis of the rejection to claims 7, 9, and 10, which ultimately depend on claim 6 is also now obviated. Applicant respectfully requests removal of the rejection to these claims.

With respect to claims 17 and 20, representative claim 17 now recites in relevant part:

> A method to process in parallel on a plurality of processors, a plurality of packets in a network which comprise a micro-flow, the method comprising
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> . . . determining whether a first packet in the plurality of packets comprising the micro-flow is currently being processed when a subsequent packet of the plurality of packets comprising the micro-flow is received;
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> responsive to determining that the first packet in the plurality of packets is currently being processed . . .

The claim has been amended to appropriately clarify and broaden the scope commensurate with which Applicant believes he is entitled. In particular, the preamble has been amended to now clarify that a micro-flow comprises a plurality of packets. In addition, the preamble has been amended to remove at this time the limitation of "variable time processes in parallel." However, Applicant does not concede to surrendering claim scope involving such limitation and reserves the right to reintroduce such limitation in appropriate context within these or other claims at any time during prosecution.

In addition, claim 17 has also been amended to recite that the process determines whether a packet among a plurality of packets of a micro-flow is being processed when a subsequent packet from the same micro-flow is received and then in response to the first

packet being processed taking the appropriate steps as further recited within the claim. Applicant respectfully submits that these amendments now obviate the basis for the rejection to claim 17, as well as claim 20. Therefore, Applicant requests removal of the basis for the rejection to these claims.

Response to Rejection Under 35 USC 102(e)

In the 4th paragraph of the Office Action, Examiner rejects claims 6-8 under 35 USC § 102(b) as allegedly being anticipated by U.S. Patent No. 6,430,184 to Robins et al. ("Robins"). This rejection is now traversed.[1]

Claim 6 recited, inter alia, a method for performing variable time processes in parallel on a plurality of ordered incoming packets, on a plurality of processors, the method comprising:

> assigning each of the plurality of ordered incoming packets to one of the plurality of processors, the packets comprising at least a portion of a micro-flow;
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> pre-processing each of the plurality of ordered incoming packets to determine whether processing on a previous packet is in progress, the previous packet comprising at least a portion of the micro-flow; and
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> processing each of the plurality of ordered incoming packets on the a processor of the plurality of processors to which the ordered incoming packet is assigned, in response to completion of processing of the previous packet.

The claimed invention beneficially assigns each incoming packet of a micro-flow to one of a plurality of processors, pre-processes those packets to determine if processing on a previous packet from the micro-flow is already in progress, and thereafter processes the incoming packets once previous packet completes processing. Hence, the claimed invention

[1] Applicant notes that Examiner makes reference to U.S. Patent No. 6,430,184 as the "Robinson" reference in the Office Action. However, this reference is to Robins et al. There is no other reference in the file history to "Robinson." Therefore, Applicant will understand the reference to "Robinson" to mean "Robins."

beneficially provides for maximum processor utilization while maintaining packet order for processing, which increases throughput.

Robins fails to disclose Applicant's claimed invention. The relay engine (RE) 40 referenced by Examiner has a primary function to:

> examine canonicalized packet headers received at interface 74 from the QM 30 and to determine rapidly whether the packet belongs to a known flow and to provide instructions accordingly on interface 75 for appropriate scheduling (quality of service). A CPU Core 387 (implemented with the ARC processor) contains an instruction cache 386 and a data cache 385 and communicates with the Code and Data DRAM 42 through the DRAM Interface 384 (which also accepts instructions from the BE 50 over a low speed bus 62 and the DMA 383 at initialization).

See Robins, 7:8-18. However, this passage in Robins merely points to a conventional process of associating a packet with a flow. There is no disclosure (or suggestion for that matter) of assigning each of the plurality of ordered incoming packets to one of the plurality of processors, the packets comprising at least a portion of a micro-flow as Applicants claim. Further, Robins in general is silent as to assigning packets in a micro-flow to particular processors. Rather, it simply refers to a conventional process of preparing flows for transmission across nodes in a network using conventional packet header information. See, e.g., Id., 2:57-65.

Moreover, the pre-processing disclosed in Robins is specifically to prepare the flow for transmission. Specifically,

> String Compare Coprocessor 389 is used to aid the pattern recognition used to match a packet and flow. Generally, a canonicalized packet header entering the RE 40 is pre-processed by the Hash Preprocessor 399 in parallel with being MUXed into Data FIFO 394 by MUXIn 394. The results of the parallel hashing are placed in Hash FIFO 393 and compared by the Hash Lookup Engine 392 with contents of the on-board L1Cache of the Hash Table (of known hashes of header information associated with particular flow characteristics) 391. If no match is found in the L1 Cache 391, the Hash Lookup Engine will look to the entire Hash Table stored in Lookup SRAM 45, accessed

> through SR Interface and Arbitrator 388. Trie Search Coprocessor 390 is used to find the proper flow parameters in situations (discussed below) where the fast pattern matching is not appropriate or fails.

Id., 7:18-34. This passage describes the relay engine 40 in Robins placing data packets in an appropriate order prior to transmission by using a hashing process to match header information with other received header information that has also been hashed and stored in a hash table. However, this is not what Applicant claims.

The pre-processing in Applicant's claimed invention provides for each of the plurality of ordered incoming packets to determine whether processing on a previous packet from the same micro-flow is in already in process. Hence, the claimed invention beneficially allows processing on a micro-flow to be in progress, while maintaining order even after assignment of the new micro-flows to particular processors. Further, the reference in Robins to col. 8, lines 6 to 36 is equally silent as to these claimed features. Rather, the reference to "circuit" in this section merely describes a logical connection for preserving ordering of a packet, which is conventional, but discloses nothing else.

Continuing with Robins, at col. 7, line 39 to col 8 line 5, it basically discloses within this section that

> operation of the preferred embodiment of the invention from the queue management point of view. Data on MOM Receive Ports 15' are directed into the QM Main Receive FIFO 330. Also enqueued are data from WAN (T1 and POTS) port receive queues 69' processed under protocols 66' and under the direction of DAD Management 66" into a DAD Ethernet transmit queue 348' to appear on a MOM receive port 348. Data cells in the Receive FIFO 330 are placed in the main system packet memory DRAMs 35 and 36 while the canonical headers are forwarded in a FIFO 394 to the QM 30 where FastPath.TM. processes are applied to enable appropriate queueing of packets on per flow, per priority and per port queues 332 (static priority, as discussed below) and 333 (weighted robin priority, as discussed below) to be transmitted to the MOM Transmit Ports 24' (or the DAD 66 to be distributed on circuit queues 350 for further distribution to T1 and POTS Port Transmit Queues 69") for transmission.

Id., 7:29-56; Fig. 5. There is no disclosure (or suggestion for that matter) of "processing each of the plurality of ordered incoming packets on the a processor of the plurality of processors to which the ordered incoming packet is assigned . . ." as Applicant claims. The passage simply notes that once packets are ordered they can be transmitted out along appropriate ports for the flow.

Thus, for at least the reasons set forth above, Robins does not disclose (or suggest) Applicant's claimed invention so that claim 6 is now patentably distinguishable. Applicant respectfully requests reconsideration and removal of the rejection to claim 6 and allowance of this claim at this time. Further, claims 7 and 8 depend upon claim 6 and are also patentably distinguishable over Robins for at least the reasons set forth above.

Response to Rejection Under 35 USC 103(a) in View of Robinson

In the 6th paragraph of the Office Action, Examiner rejects claims 9-10, 17, and 20 under 35 USC § 103(a) as allegedly being unpatentable in view of Robins.

The relevant portions of these claims recite, inter alia,

> determining whether a first packet in the plurality of packets comprising the micro-flow is currently being processed when a subsequent packet of the plurality of packets comprising the micro-flow is received;
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> responsive to determining that the first packet in the plurality of packets is currently being processed:
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> not starting processing of the subsequent packet of the plurality of packets;
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> at a later time determining whether the first packet in the plurality of packets is currently being processed;
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> responsive to determining that the first packet in the plurality of packets is not currently being processed, starting processing of the subsequent packet of the plurality of packets; and
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> processing each of the plurality of packets on a processor of the plurality of processors to which the packet is assigned.

As previously noted, the claimed invention pre-processes packets to determine if a processing on a previous packets from a same micro-flow is already in progress, and if so, processes the incoming packets once previous packets of the micro-flow complete processing. Hence, the claimed invention maintains packet order for processing, while increasing processor utilization, and in turn, throughput.

Examiner correctly points out Robins fails to disclose Applicants claimed inventive features. However, such features are also not obvious in view of Robins. Citations to col. 15, line 65 to col. 16, line 15 merely point to a mechanism to track cells when canonical headers are unavailable for use to track packet order; and to col. 19, lines 54-57 point to use of conventional hash look up tables to determine order of processing. There is no disclosure or suggestion about how Robins would even contemplate processing of subsequent packets of a micro-flow, which are assigned to a processor of a plurality of processors, in response to an in-progress processing of a packet from the same micro-flow.

In addition, as Examiner is well aware, of the burden to establish a prima facie case of obviousness. Examiner can satisfy this burden "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references" in the manner suggested by Examiner. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "[E]lements of [patents and/or publications] cannot be combined when there is no suggestion of such combination anywhere in those patents [and/or publications]...; and a court should avoid hindsight..." (emphasis added; annotations within square brackets). Panduit Corp. v. Dennison Mfg. Co., 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), citing ACS Hospital Systems, Inc. v. Montefiore Hospital, 220 USPQ 929, 933 (Fed. Cir. 1984), and W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983). *See also* Uniroyal Inc. v.

Rudkin-Wiley Corp., 5 USPQ2d 1434, 1438-1441 (Fed. Cir. 1988). In fact, it is impermissible to use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. In re Fine, 5 USPQ2d at 1600. Here, Applicant notes that nowhere in Robins is there even a mention of "sequential processing" as Examiner states Robins teaches leaving a question of whether hindsight may be an issue. Robins simply does not contemplate processing in a matter as Applicant's claims recite.

Thus, Applicant respectfully requests reconsideration and removal of the rejection to claims 10, 17, and 20 as these claims also are patentably distinguishable over the cited references. Applicant also requests allowance of these claims at this time.

Conclusion

In sum, Applicant respectfully submits that claims 6-10, 17, and 20, as presented herein, are patentably distinguishable over the cited references (including references cited, but not applied). Therefore, Applicant requests reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicant respectfully invites Examiner to contact Applicant's representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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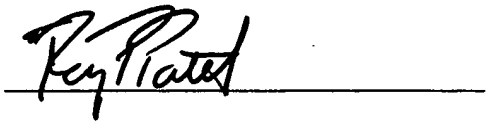
Date: August 19, 2004 By: 

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